University of Mumbai

Examinations Summer 2022

Program: Electronics and Telecommunication Engineering

Curriculum Scheme: Rev2019

Examination: SE Semester III

Course Code: ECC302 and Course Name: Electronic Devices and Circuits

Time: 2 hour 30 minutes Max. Marks: 80

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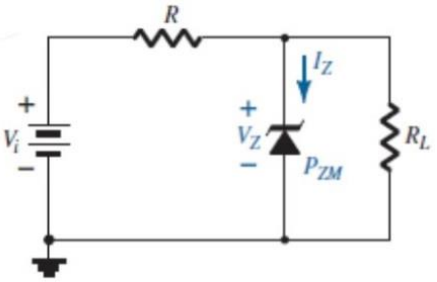
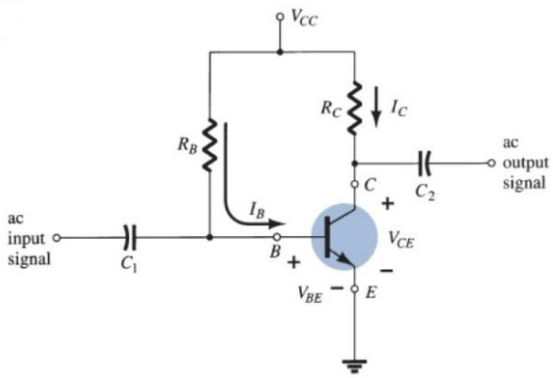
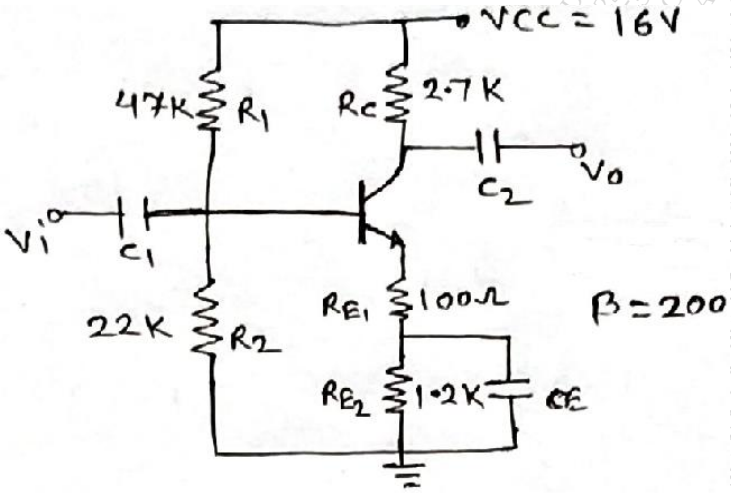
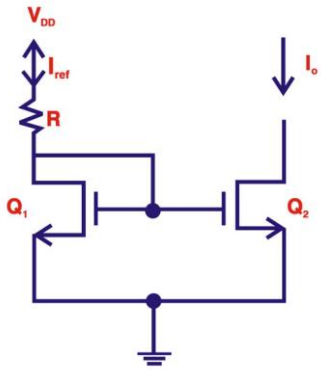
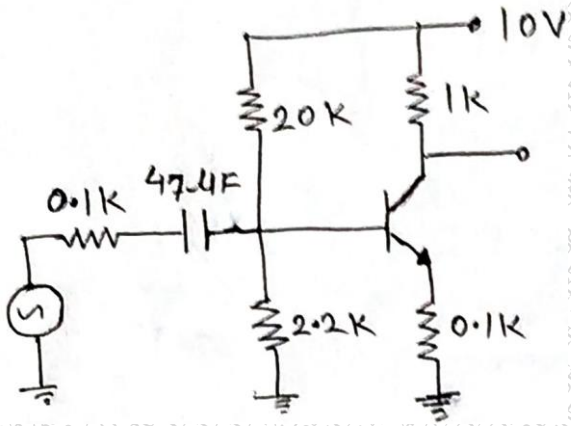
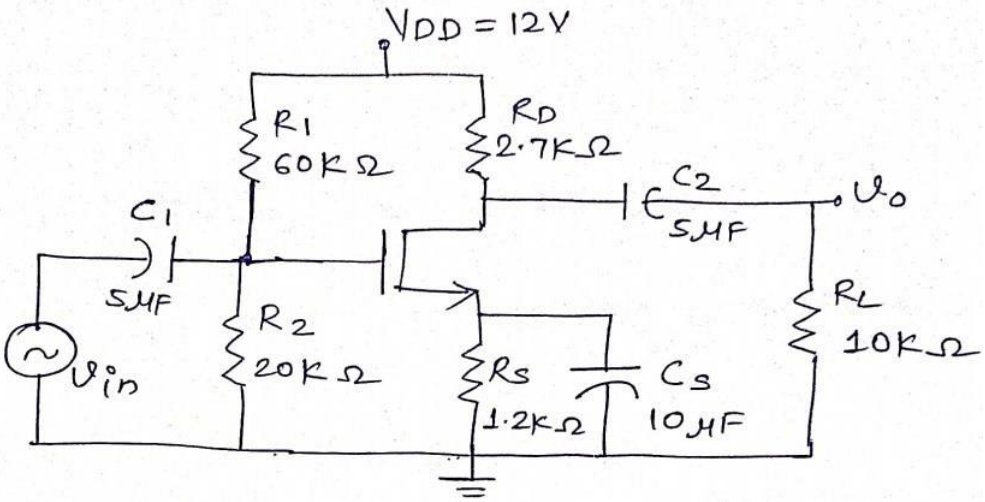
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	The reverse saturation current of a transistor increases with the increase of temperature at the rate of:
Option A:	doubles in value for every 1°C increase in temperature
Option B:	doubles in value for every 25°C increase in temperature
Option C:	doubles in value for every 10°C increase in temperature
Option D:	quadruples in value for every 100°C increase in temperature
2.	Calculate the voltage across R_L. V_i = 9 V, V_Z = 3 V, R=6.8 KOhms, R_L=2.2 KOhms 
Option A:	3 V
Option B:	2.2 V
Option C:	9 V
Option D:	4.4 V
3.	For a JFET self bias circuit, if the source resistance is increased keeping all other parameters constant, what is the effect on the operating point?
Option A:	Can't change Source resistance
Option B:	Remains same
Option C:	It moves towards ID = IDSS, VGS = 0
Option D:	It moves towards ID = 0, VGS = VP
4.	Adding a Resistor between emitter of BJT and Ground terminal of a CE BJT amplifier _____
Option A:	Decreases the stability of the amplifier
Option B:	Improves the stability of the amplifier
Option C:	Increases the Gain of the amplifier
Option D:	Has no effect
5.	To operate as an amplifier, BJT and MOSFET should operate in _____& _____ regions respectively
Option A:	Active and Saturation

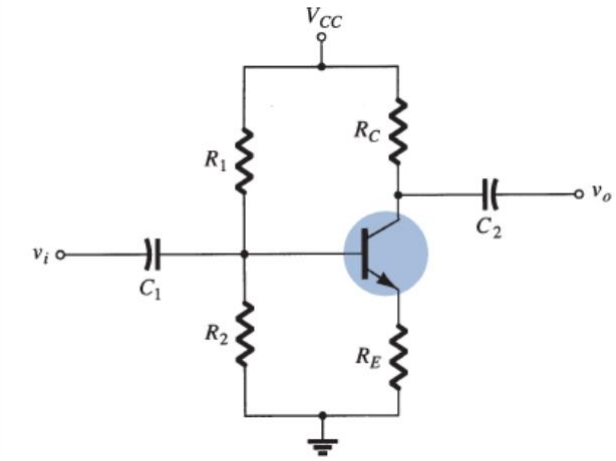
Option B:	Saturation and linear
Option C:	Cutoff and Linear
Option D:	Saturation and Cutoff
6.	For the fixed bias circuit shown, calculate the small signal input impedance, Zi in Ohms. Beta=120. R_B=240KΩ, R_C=1.2KΩ, V_CC = 12 V, V_BE = 0.7 V, 
Option A:	1.2 KOhm
Option B:	240 Kohm
Option C:	551 ohm
Option D:	1 KOhm
7.	High cutoff frequency of an amplifier depends on
Option A:	Output Coupling capacitor
Option B:	bypass capacitor
Option C:	Input Coupling capacitor
Option D:	Parasitic capacitor
8.	For a direct coupled amplifier, if f_H = 200 KHz then calculate the bandwidth of the amplifier.
Option A:	1 KHz
Option B:	100 KHz
Option C:	200 KHz
Option D:	400 KHz
9.	If output is measured between two collectors of transistors, then the Differential amplifier with two input signal is said to be configured as
Option A:	Dual Input Balanced Output
Option B:	Dual Input Unbalanced Output
Option C:	Single Input Balanced Output
Option D:	Single Input Unbalanced Output
10.	Power amplifier directly amplifies _____
Option A:	Voltage of signal but not Current
Option B:	Current of the signal but not Voltage
Option C:	Power of the signal but not Voltage and Current
Option D:	Voltage, Current and Power of the signal

Q2.	Solve any Two Questions out of Three 10 marks each
A	Determine the following for the network given below Fig. 1 Voltage gain, Current gain, input impedance and output impedance  Fig. 1
B	With neat diagram derive the efficiency of transformer coupled class –A power amplifier? State its uses.
C	Explain construction and working of n-channel E-MOSFET with output characteristics

Q3	
A	**Solve any Two** **5 marks each**
i.	For a Class B amplifier providing an 18 V peak signal to a 20 Ω load (Speaker) and a power supply of VCC = 20 V, determine the output power, input power and efficiency.
ii.	Why should be Rc as large as possible in design of CE amplifier?
iii.	Explain Zener diode as a voltage regulator.
B	**Solve any One** **10 marks each**
i.	Let V_{DD} = 5V, $V_{TH,1}$ = 1V, $k_{n,1}'$ = 20μA/V^2 and R = 1KΩ. What should be $(W/L)_1$ needed for creating I_{ref} = 1mA? What should be $(W/L)_2$ if we want I_o = 7mA, 10 mA and 15 mA? Refer Fig. 2  Fig. 2

ii.	For the circuit shown in Fig. 3, the transistor parameter are V_{BE} (on) = 0.7 V, β = 200, VA = ∞, i. Derive the expression for lower cutoff frequency due to input coupling capacitor. ii. Determine lower cut-off frequency and voltage gain  Fig.3

Q4	Solve any Two	10 marks each
A	Explain the operation of a Differential amplifier for common mode signals and differential input signals. Also explain CMRR.	
B	Determine f_L, f_H, f_T.  Given: $K_n' = \mu_n C_{ox} = 100\,\mu A/V^2$, $V_{Tn} = 0.5\,V$ $W = 1.8\,\mu m$, $L = 180\,nm$, $\gamma_d = \infty$ $C_{gd} = 2$ pF, $C_{gs} = 4$ pF, $C_{ds} = 0.5$ pF, $C_{W_i} = 5$ pF, $C_{W_o} = 6$ pF	

C	Design a voltage divider bias circuit operating at (V_{CEQ} = *12 V*, I_{CQ} = *2 mA*) for S(I_{CO}) ≤ 5. Given: β = 100, V_{CC} = 20 

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Examinations Summer 2022

Time: 2 hour 30 minutes Max. Marks: 80

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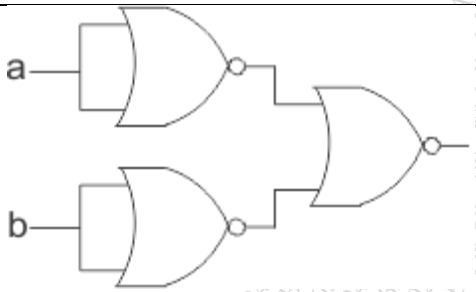
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Which of the following gates is known as Universal Gate?
Option A:	XOR
Option B:	NOT
Option C:	AND
Option D:	NAND
2.	 If Y is the output for the above figure, determine the output expression for the given logic diagram.
Option A:	Y=AB
Option B:	Y=A'B'
Option C:	Y=A+B
Option D:	Y=A⊕B
3.	Which of the following law is not correct?
Option A:	A + 1 = 1
Option B:	A + A = A
Option C:	A.A = A
Option D:	A + A'= 0
4.	Which of the following is NOT considered for forming groups in K-map?
Option A:	Rolling
Option B:	Diagonal
Option C:	Vertical
Option D:	Horizontal
5.	Which of the following is not an example of sequential circuit?
Option A:	Flip flop
Option B:	Counter
Option C:	Magnitude Comparator
Option D:	Shift Register
6.	2's complement representation of 23 is_____.
Option A:	1101000
Option B:	1101001
Option C:	1100100
Option D:	1101010

7.	A ____is composed of a group of flip flops to store a group of bits.
Option A:	Counter
Option B:	Decoder
Option C:	Demultiplexer
Option D:	Register
8.	Shift register application includes_____
Option A:	Ring counter
Option B:	Decade counter
Option C:	Bounce elimination switch
Option D:	BCD to 7-segment decoder
9.	Which of the following is true about PAL?
Option A:	Both OR & AND array are programmable.
Option B:	AND array is programmable & OR array is fixed.
Option C:	AND array is fixed & OR array is programmable.
Option D:	Both OR & AND array are fixed.
10.	A declaration of a module's inputs and outputs in VHDL is _____
Option A:	VHDL entity
Option B:	VHDL architecture
Option C:	VHDL Interface
Option D:	VHDL Conceptual Model

Q2 (20 Marks)	**Solve any Four out of Six** **5 marks each**
A	Perform the given conversion, $(FBE6)_H = (?)_{10} = (?)_2 = (?)_8$
B	What are universal gates? Why they are called universal gates? Justify with example.
C	Write basic laws for Boolean algebra.
D	Give Comparison for TTL and CMOS logic families.
E	Compare decoder and demultiplexer.
F	List different types of flip-flops with their characteristic equations.

Q3 (20 Marks)	**Solve any Two Questions out of Three** **10 marks each**
A	Get the minimal expression using Quine McClusky method for the following logic function: $f(A,B,C,D) = \Sigma m\,(1, 3, 5, 8, 9, 11, 15) + d(2,13)$
B	Design & implement 4-bit Binary to Gray code converter.
C	What is modulus of a digital counter? Design a synchronous counter with irregular binary count sequence 1----2----5----7. Use JK flips flop.

Q4 (20 Marks)	**Please delete the instruction shown in front of every sub question**
A	**Solve any Two** **5 marks each**

i.	Convert D flip flop to T flip flop
ii.	Write a VHDL code for 4:1 MUX.
iii.	Give classification of semiconductor memories and explain about DRAM in brief.
B	**Solve any One** **10 marks each**
i.	Draw the block diagram of BCD adder using IC 7483 and show with example the addition of two BCD numbers
ii.	Explain different application of sequential circuits with relevant diagrams.

University of Mumbai

Examinations Summer 2022

Program: **Electronics and Telecommunication Engineering**

Curriculum Scheme: Rev-2019

Examination: SE Semester III

Course Code: ECC304 and Course Name: Network Theory

Time: 2 hour 30 minutes Max. Marks: 80

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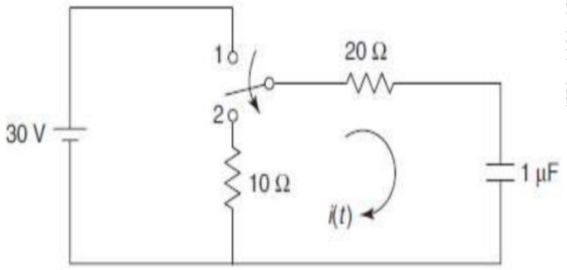
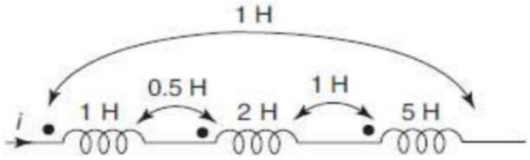
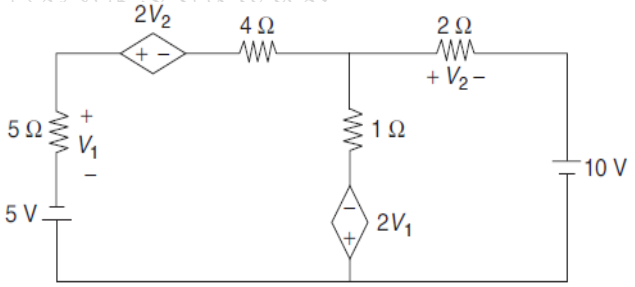
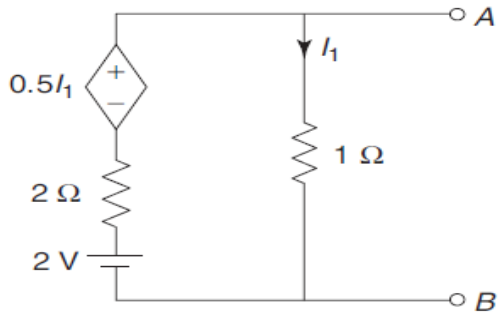
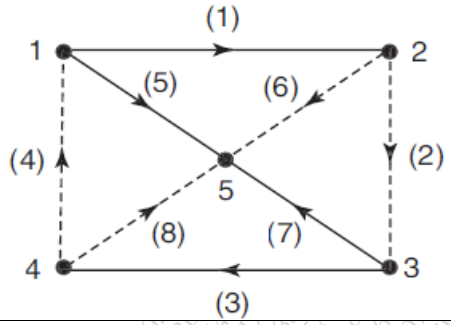
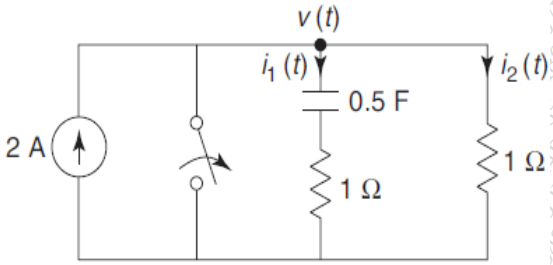
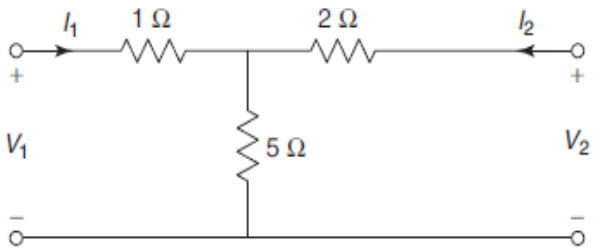
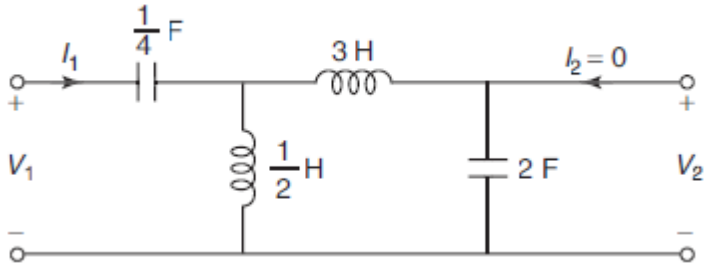
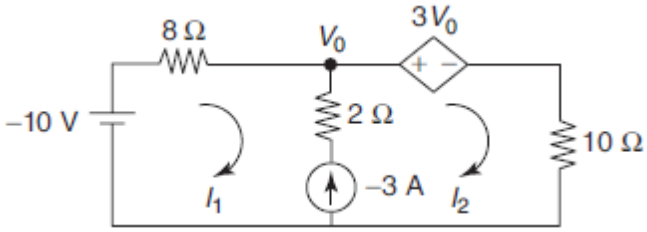
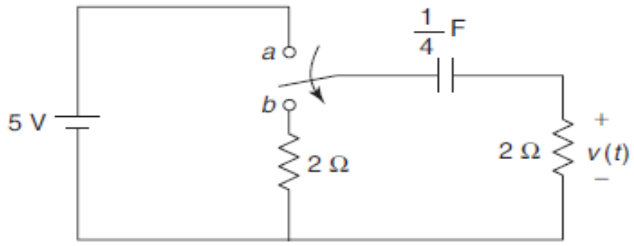
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	According maximum power transfer theorem which of the following option is true?
Option A:	Rth < Rl
Option B:	Rth > Rl
Option C:	Rth = Rl
Option D:	Rth = 0
2.	Which Of the following is property of Positive Real Function?
Option A:	The poles and zeros of a positive real function cannot have positive real parts
Option B:	Only simple poles with real negative residues can exist on the jw-axis
Option C:	The poles and zeros of a positive real function can have positive real parts
Option D:	The sum of two positive real functions is not a positive real.
3.	Which of the following is the Transfer Impedance function?
Option A:	V1 / V2
Option B:	I2 / V1
Option C:	I2 / I1
Option D:	V1 / I2
4.	Find the voltage across capacitor and current i(t) at $t = 0^+$ respectively. 
Option A:	0V, -1A
Option B:	30V, -1A
Option C:	30V, 0A
Option D:	0V, 0A
5.	Find the equivalent inductance of given network. 
Option A:	10 H
Option B:	12 H
Option C:	13 H
Option D:	15 H
6.	Which of the following property satisfies the symmetrical criteria of two port network?

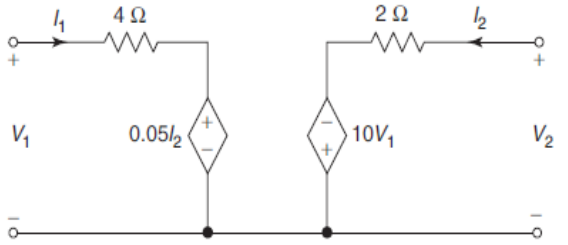
Option A:	h11 h22 - h12 h21 = 1
Option B:	AD-BC=1
Option C:	Z11 Z22 -Z12 Z21 = 1
Option D:	Y21= Y12
7.	The reduced incidence matrix is given below, find the total number of possible trees. $A=\begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 \\ 0 & -1 & 1 & -1 & 0 & 0 \\ -1 & 0 & -1 & 0 & -1 & 0 \end{bmatrix}$
Option A:	12
Option B:	14
Option C:	20
Option D:	16
8.	For t = 0^- i.e. At initial condition inductor and capacitor are___ and ___ respectively.
Option A:	Short circuited , Open circuited
Option B:	Open circuited , Short circuited
Option C:	Short circuited , Short circuited
Option D:	Open circuited , Open circuited
9.	If the graph consists of 4 nodes and 6 branches then the number of twigs and number of links are ------ and ------ respectively.
Option A:	5, 5
Option B:	4, 4
Option C:	3, 4
Option D:	3, 3
10.	_____ theorem states that any two terminals of network can be replaced by equivalent Voltage source and an equivalent series resistance.
Option A:	Maximum power Transfer
Option B:	Thevenin's theorem
Option C:	Norton's theorem
Option D:	Duality theorem

Q2 (20 Marks)	**Solve any Four out of Six** **5 marks each**
A	Find the Mesh Currents in the Network Shown- 
B	Find the Norton's equivalent Network-

	
C	For the Graph shown ,write the complete incidence matrix and tiset matrix- 
D	In the network, switch is closed for a long time and at t=0 switch is opened. Determine the current through the capacitor – 
E	Find the transmission parameter for the network shown- 
F	Test whether, F(s) is a positive real function. $F(s) = \frac{s+3}{s+1}$

Q3 (20 Marks)	**Solve any Two Questions out of Three** **10 marks each**
A	Find the Network Functions $\frac{V1}{I1}$, $\frac{V2}{V1}$ and $\frac{V2}{I1}$ for the Network -

	
B	In the network Shown Find I_1 and I_2 – 
C	In the Network shown, the switch is shifted to position b at t = 0. Find V(t) for t > 0. 

Q4. (20 Marks)	**Solve any Two Questions out of Three** **10 marks each**
A	Determine Z and Y parameters of the Network shown- 
B	Determine the Foster form I and Foster Form II of realisation of RC impedance function- $$Z(s) = \frac{(s+1)(s+3)}{s(s+2)(s+4)}$$
C	For the Network shown, write down the f –cutset matrix and obtain the Network equilibrium equation in matrix form using KCL.